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# STACKING TECHNOLOGY FOR A SPACE CONSTRAINED MICROSYSTEM

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## ABSTRACT

In this paper we present a stacking technology for an integrated packaging of an intelligent transducer which is formed by a micromachined silicon transducer and an integrated circuit chip. Transducer and circuitry are stacked on top of each other with an intermediate chip in between. The bonding of the transducer and the intermediate chip is done by flip chip solder bump bonding. The bonding between the above two-layer stack and the circuit chip is done by conductive adhesive bonding combined with gold studs. We demonstrate the stacking technologies on passive test chips rather than real devices and report on technological details.

## INTRODUCTION

Realization of multifunctional microelectromechanical systems (MEMS) by integrating individual chips and devices is gaining more and more attention today. Additional to a high performance and package density, volume and weight become important design factors. Small volume systems are especially required for bio-medical, space and aircraft industries. In such space constrained applications the integration should preferably be done by stacking rather than conventional planar arrangements. Besides the reduction in size, stacked systems benefit from shortened electrical interconnections, thus increasing operation speed and reducing parasitic loads. Furthermore, if all components to be integrated have a high yield and the same footprint area stacking on wafer level becomes possible.

Stacking as a packaging concept for boards but also bare dies has already been practised for many years. For a review of different stacking technologies see [1]. Integration of circuitry wafers for memory stacks was proposed in [2, 3], where the concept is based on wafer through-hole frontside to backside interconnections.

In contrast, we present a stacking technology for the integrated packaging of an intelligent transducer which is formed by a micromachined silicon transducer and an integrated circuit chip. The reason for choosing a hybrid approach is the separate fabrication of the individual devices. Thereby we faciliate device processing and minimize compromises on performance. The transducer chips, such as resonant gyroscopes, accelerometers and condenser microphones, can carry all kinds of sensitive, movable, and fragile parts and the surface finish can be very complicated including protruding structures. The integrated circuit is based on commercial CMOS technology. Therefore, assembly technologies have to be adjusted to the particular features of the MEMS components and to the metallization used in standard CMOS process. Transducer and circuitry are stacked on top of each other with an intermediate layer in between them, see Fig. 1. The intermediate layer has several functions which we will point out in the following section.

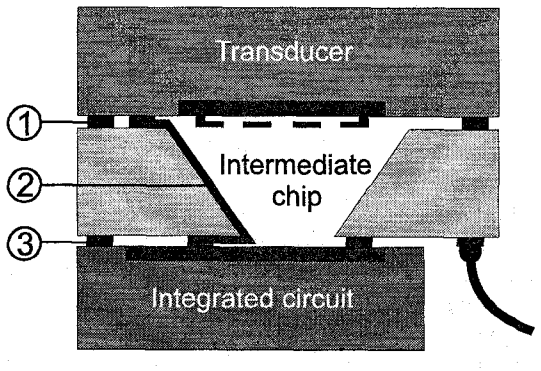


*Figure* 1: *Topology of the stacked intelligent transducer. The numbers indicate the different electrical interconnections required:* **1:** *between the transducer chip and the intermediate chip,* **2:** *through the intermediate chip,* **3:** *between the intermediate chip and the circuit chip.*

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# ELECTRICAL INTERCONNECTS

The electrical interconnects indicated in Fig. 1 were chosen to be solder bump bonding, multiple feedthroughs and conductive adhesive bonding, respectively. Hereby, attention was paid to the special features of the individual parts and their application. A maximum allowable processing temperature of approximately 400° C applies to all of them.

### Solder bonding

Intermediate layer and transducer chip are electrically interconnected using flip chip solder bump bonding. With this technique we were able to combine single interconnects with a sealing ring in one process step [4], see Fig. 2. The sealing ring improves the mechanical stability and ensures a controlled access of the ambient to the transducer. The bonding process needs to be fluxless because of the delicate features of the transducer. In contrast to alternative fluxless processes [4, 5, 6] our technology does not need pre-reflow of the solder bumps nor reducing gases during the bonding process [7]. This will be discussed in more detail below.

### Intermediate layer

The intermediate layer serves several purposes. It does re-routing of the interconnections between transducer and circuit. It provides the delicate transducer surface with a proper front chamber and a controlled ambient access. Besides, it provides the stack with bonding pads for electrical interconnections to the outside world, see Fig. 2. The intermediate layer is made of silicon to avoid any mechanical loading of the transducer due to mismatch in thermal expansion. The interconnect metallization has to be wettable for the used solder and stable during operation. Furthermore, it must be provided with a solder dam. The geometrical dimensions of the interconnect lines depend on their functions, whether they are signal, ground or power lines.

### Conductive adhesive bonding

The bonding between the above stack and the integrated circuit chip is done by conductive adhesive bonding. This is the only technique that allows flip-chip bonding of single dies with low bonding forces. The process uses gold studs dipcoated in conductive adhesive [8]. This technique has the advantage to be compatible with the aluminum metallization, thus avoiding any post-processing on the pads of the circuitry chips other than the stud bumping. The gold studs are used since adhesives usually cannot form

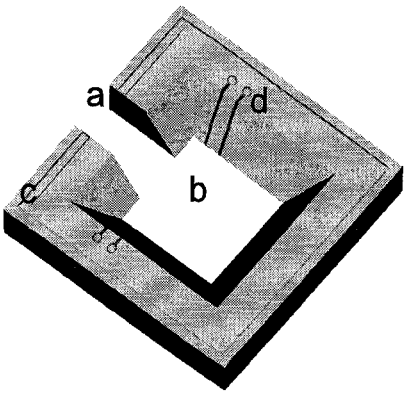


*Figure 2: Schematic drawing of an intermediate chip with the upper side being the transducer side.* **a** *indicates the controlled ambient access,* **b** *the front chamber,* **c** *the sealing ring, and* **d** *the electrical frontside to backside interconnections.*

strong bonds to the aluminum metallization without pre-treatment of the bonding pads [9]. The curing temperature of the adhesive is well below the soldering temperature, ensuring integrity of the solder bump bond.

# EXPERIMENTAL

In the following we describe the processing of the intermediate layer as well as the bonding steps in detail. In our experiments we used passive test chips rather than real devices and a glass chip instead of the silicon transducer chip. Also, in this investigation the formation of the solder bumps is done on the glass chip (on wafer scale) rather than on the intermediate layer, see Fig. 3.

### Intermediate layer

The intermediate layer is made of double side polished (100) silicon with a wafer thickness of 350 $\mu$m. The through-holes were etched anisotropically in 28 wt% potassium hydroxide using either thermal oxide or silicon-rich silicon nitride as etch mask. After removing the etch mask a 2 $\mu$m thick thermal oxide was grown to serve as a dielectric layer. Next, a titanium layer with a thickness of 3000 Å was deposited by e-beam evaporation. This layer acts as plating base for the subsequent photoresist deposition. The used photoresist is the electrodepositable photoresist Eagle 2100 ED manufactured by Shipley. For details concerning photoresist processing see [10, 11], for lift-off capability see [12]. The photoresist was patterned on both sides by exposure through a reticle mask to UV light in a standard dou-

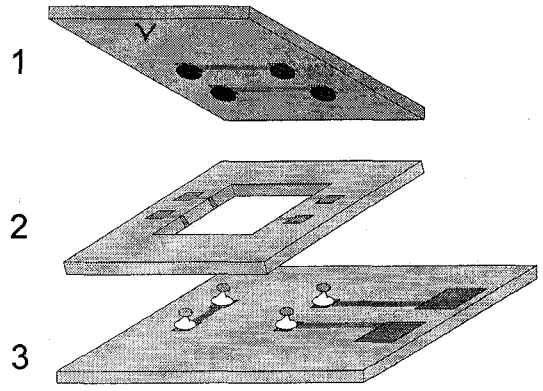


*Figure 3: Assembly of chips in this investigation:* **1:** *glass chip with under bump metallization and solder bumps,* **2:** *silicon intermediate chip with multiple frontside to backside interconnections and top surface metallization,* **3:** *silicon chip with aluminum metallization, gold stud bumps and conductive adhesives. The interconnection scheme in this figure was designed for electrical characterization.*

ble sided mask aligner. The interconnect lines on the frontside mask above the sidewalls are tapered in order to counteract diffraction effects due to the large projection length between the mask and the bottom of the through hole. After resist development the exposed titanium was etched in 1% hydrofluoric acid. The interconnect metallization consisting of 300 Å of chromium and 2000 Å of platinum was e-beam evaporated and lifted off by dissolving the remaining photoresist in acetone. Finally, the remainder of the titanium plating base is etched in 5% hydrofluoric acid. An intermediate chip realized in silicon is shown in Fig. 4.

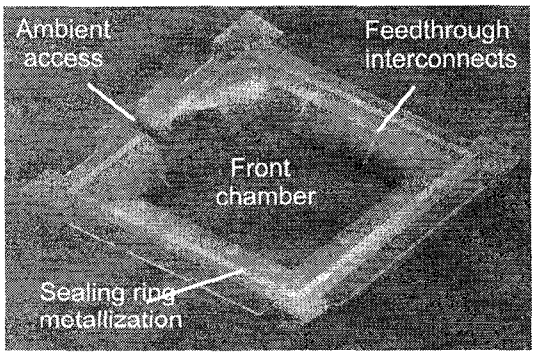


*Figure 4: Transducer side of the intermediate chip realized in silicon.*

The linewidth of the interconnect lines is 30 $\mu$m. The bond pads have an octagonal shape and outer dimensions of 100 $\mu$m. The sealing ring metallization has a width of 100 $\mu$m. The ambient access hole is realized by using different types of convex corner compensation structures during anisotropic etching. For the electrical characterisation of the interconnect lines a design as shown in Fig. 5 was used.

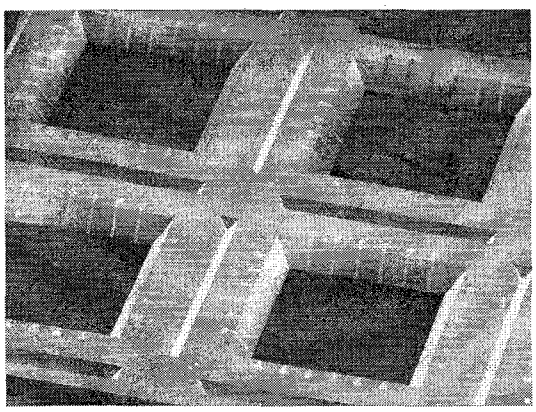

*Figure 5: Array of intermediate test chips as sketched in Fig. 3.*

Next, a solder dam is realized at the transducer side to prevent the molten solder to spread further onto the interconnect lines during soldering. For this purpose we chose an approximately 2000 Å thick undoped PECVD silicon dioxide. To open contact holes for the bonding pads we used the electrodepositable photoresist again. For selectivity reasons, the resist plating base consists of 200 Å of chromium and 1000 Å of gold. The patterned photoresist serves as mask in the subsequent etching processes. The gold was etched in a potassium iodine solution, the chromium was etched in a cerium(IV)-sulfate/nitric acid solution, and the PECVD glass was etched in 5% HF. Next, the photoresist was removed and the plating base was etched using the above etchants. Fig. 6 shows a close up of a bond pad provided with a solder dam.

### Flip chip solder bump bonding

For the solder bump bonding we used glass dies because they allow to observe solder reflow and self-alignment during the bonding process. An under bump metallization (UBM) was deposited and structured by lift-off using standard photoresist processing. The UBM consists of 3000 Å of platinum as wettable surface and 200 Å of chromium or titanium as adhesion layer and diffusion barrier. Platinum was chosen because it is compatible with the transducer processing (high temperature processes) and has a high leach resistance [13]. A PECVD silicon dioxide was deposited and patterned to serve as a solder dam similiar to the solder dam on the intermediate layer. Next, we deposited the solder bumps by

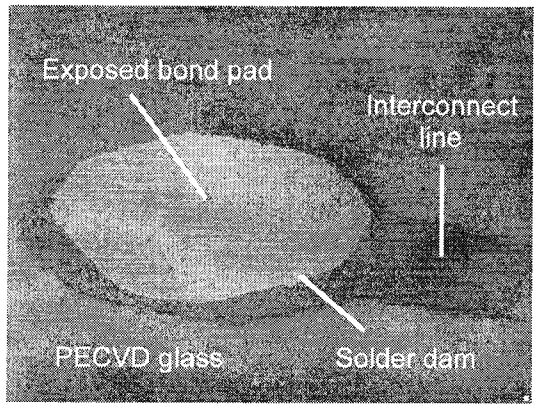


*Figure 6: Close up of a bond pad provided with a PECVD silicon dioxide solder dam.*

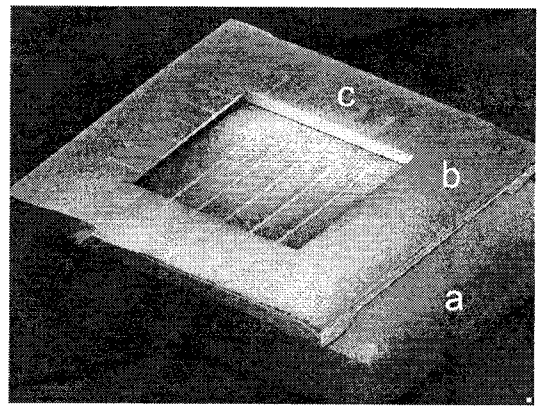


*Figure 7: Intermediate chip with teststructures solder bonded to a glass chip.* **a:** *glass chip (emulating the transducer chip) with solder bumps,* **b:** *intermediate chip with vertical feedthroughs and top surface metallizations on top and bottom side,* **c:** *Electrical frontside to backside interconnections termination for further stacking.*

e-beam evaporation and structured them by lift-off using a thick photoresist mask with negative sidewalls [7]. For our investigation we used two types of solder, pure tin (melting point $T_m$ = 232 °C) and eutectic SnAg3.5 ($T_m$ = 221 °C). The bump height as deposited was approximately 15 $\mu$m.

Since MEMS components, as already stated, contain fragile movable parts, membranes and/or sensitive surfaces fluxes cannot be applied to promote wetting and prevent re-oxidation during the soldering. Using as-deposited solder bumps and in-situ reflow it was possible to solder in an ambient with reduced partial pressure of oxygen ($10^{-5}$ Pa). When heating up the solder the bumps start to reflow and, thus break the solder oxide layer on their surface. Re-oxidation during bonding is prevented due to the low oxygen partial pressure. The bonding temperature for the experiments was 250 °C. The self-alignment of the components, which is due to surface tension forces of the molten solder could be observed in all cases within 20 sec after the melting point of the solder was reached [7]. Fig. 7 shows a solder bonded stack consisting of a glass test chip and an intermediate chip.

### Adhesive bonding

The adhesive bonding of the above two-layer stacks was done both to silicon as well as to glass dies. The glass dies were used to observe the processes and the silicon dies to demonstrate the compatibility with ASIC wafers. The metallization on these dies was aluminum in order to comply with the standard in commercial CMOS. First, gold studs were produced by mechanical bumping using a conventional ball-wedge bonder [14]. Then the gold bumps are dipped into a layer of conductive adhesive. Next, the so prepared samples are aligned to the solder bonded stack using a commercial flip-chip bonder and cured. The obtained bond is not very strong and is also sensitive to contaminants entering the small air gap between the bonded chips. Therefore the airgap is filled by a non-conductive polymer (underfiller). This underfiller has to be chosen in respect to the used conductive adhesive. In our case we have followed the instructions from two vendors (Epotek [15], Namics [16]). Usually, the underfill is supplied only at one corner or one edge and fills the whole gap due to capillary forces. Since the through-hole limits the capillary forces we applied the underfill from two sides. Finally, the underfill is cured which ensures the necessary strength and stability. In our experiments we used two adhesive systems with different curing times. Detailed information on these systems is proprietary. Fig. 8 shows a cross-sectional view of adhesive bonds in a silicon stack.

Fig. 9 shows a complete stack of an intermediate chip and two test chips realized by applying the technologies described above.

## DISCUSSION

Electrical characterization was done according to the model shown in Fig. 10. We measured three different resistances being $R_{m_{AC}}$ = 26 Ω, $R_{m_{BG}}$ = 80 Ω and $R_{m_{DE}}$ = 25 Ω. We repeated all measurements several times with different samples. Based on these numbers we obtained for $R_{BD}$ = 27.5 Ω. Calculations using the specific resistivity of platinum and the geometrical dimensions yield the following theo-

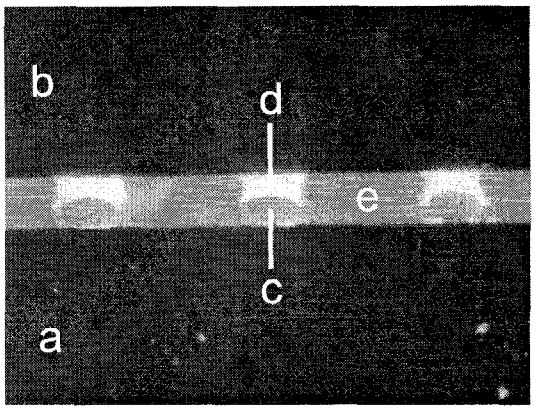


*Figure 8: Cross-sectional view of adhesive bonds.* **a:** *silicon chip carrying gold studs,* **b:** *intermediate chip,* **c:** *gold stud bump,* **d:** *conductive adhesive,* **e:** *non-conductive adhesive (underfill).*

retical resistances: $R_{c_{AC}} = 13\ \Omega$, $R_{c_{BG}} = 51\ \Omega$ and $R_{c_{DE}} = 25\ \Omega$. The differences between measured and calculated numbers can be accounted for uncertain resistances at the sharp corners of the through-hole and uncertain conditions at the bonding interfaces, which means unknown $R_{AB}$, $R_{CD}$, $R_{EF}$ and $R_{GH}$. The results presented here must be considered to be preliminary. Especially the resistances at the sharp corners as well as the contact resistances at the bond interfaces need further investigation. The high resistance in general is due to the high resistivity of platinum and the thin layers which have been deposited. For applications requiring lower resistance an additional metal layer has to be deposited underneath the platinum. The calculated parasitic capacitance of the feedthrough interconnects to the bulk silicon is 0.8 pF. This number also includes two bond pads. If the feedthrough interconnect is considered to be a part of a closed-loop system (as in a real stack) the partial self-inductance can be calculated applying closed-form formulas [17]. In our case the result is 40 nH.

Reliability demands on the stacking technologies presented here comprise corrosion resistance, fatigue life and stability of the used metallization system. From the design of our technologies, processes and materials, we however can expect a highly reliable assembly technology since
- we have no mismatch in the thermal expansion coefficients (all layers are made of silicon);
- we do not use fluxes which is the major cause for reliability degradation due to corrosion;
- we use a platinum metallization which has been proven to have a superior leach resistance among commonly applied thin film metallizations.

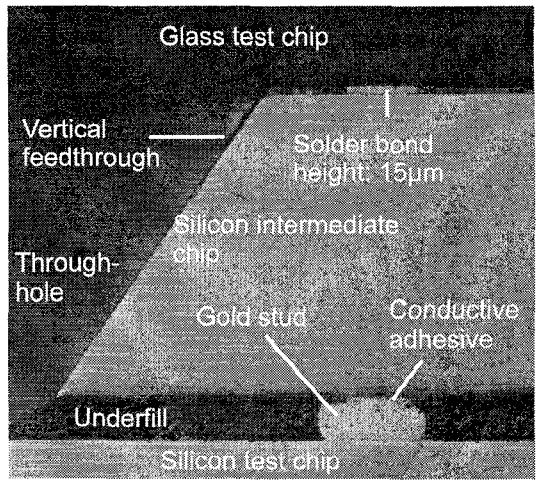


*Figure 9: Complete three-layer stack consisting of a glass test chip solder bonded to an intermediate chip with frontside to backside interconnections and a silicon test chip adhesively bonded to the above two-stack.*

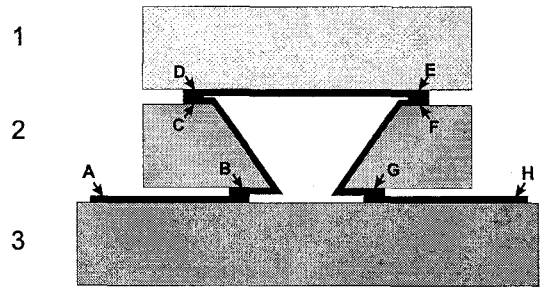


*Figure 10: Resistance model used for electrical characterization. The numbers indicate the three layers:* **1:** *glass chip with solder bumps,* **2:** *intermediate chip with feedthroughs and* **3:** *silicon chip with gold studs and adhesive. The characters indicate the different resistances.*

Future investigations include bumping of the intermediate layer rather than the transducer layer, more complex metallization schemes to reduce the resistance and stability testing.

# CONCLUSION

We have developed a stacking technology for an intelligent transducer. Our concept is based on solder bump bonding, an intermediate layer with multiple frontside to backside interconnections and conductive adhesive bonding. The solder bonding process is fluxless. The bonding is done in an ambient with reduced oxygen partial pressure using solder bumps

as deposited. The adhesive bonding is based on gold stud bumps dipcoated with conductive adhesive. Sufficient strength is ensured by an underfill. Both investigated solder types as well as both adhesive systems yielded reliable and strong bonds. Multiple frontside to backside interconnections were realized with a wettable top surface metallization. The yield of these structures is 100 %.

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